

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No.10/624,716
Filing Date July 21, 2003
Inventor.....Luan C. Tran
AssigneeMicron Technology, Inc.
Group Art Unit2812
ExaminerKennedy, Jennifer M.
Attorney's Docket No.MI22-2357
Title: Methods of Forming Semiconductor Constructions

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56.
Copies of the cited art are included with the exception of U.S. patents and published U.S.
applications (1276 OG 55). No admission is made regarding whether all the submitted
references are prior art.

Respectfully submitted,

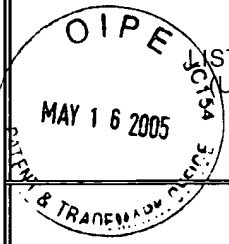
Dated: May 16, 2005

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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2357		SERIAL NO. 10/624,716	
 LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran			
				FILING DATE July 21, 2003		GROUP 2812	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,534,456	07/96	Yuan et al.			
	AB	4,985,740	01/91	Shenai et al.			
	AC	5,904,530	05/99	Shin			
	AD	US2002/0006693	01/02	Matsuda			
	AE						
	AF						
	AG						
	AH						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation Yes No
	AP	JP04105328A	04/92	Japan			Abstract
	AQ						
	AR						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AS		Wolf et al., "Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Second Edition, Lattice Press 2000, pp.12-13, 25-27.				
	AT		S.M. Sze, VLSI Technology, Second Edition, McGraw-Hill, 1988, pages 472-483				
EXAMINER				DATE CONSIDERED			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							